1. 
(1) (5%) Let $A = 30_{10} = 00011110_{2}$ and $B = 17_{10} = 00010001_{2}$. Use 2's complement addition to calculate $A - B$ and $-A - B$, and represent the answers in 2's complement.

(2) (2%) Prove the consensus theorem

$$XY + X'YZ + YZ = XY + X'Z$$

(3) (5%) Reduce the following switching function to a minimum sum-of-products form

$$F = WX'Y + (WY'X) + (Y \oplus WZ)$$

(4) (5%) Given two 3-variable Boolean functions:

$$F_1 = \prod M(0, 4, 5, 6)$$

$$F_2 = \sum m(0, 3, 4, 6, 7),$$

draw the Karnaugh maps for $F_1 F_2$ and $F_1 + F_2$.

2. (8%) 在一電視遊戲中，A 先生宣稱他和太太 B 很有默契，對所有事情的看法完全一致，而他的大兒子 C 和他看法完全相反，他的二兒子 D 是極度樂觀的人，對所有的事情都持正面看法。主持入將他們四人隔開，問同樣的一個問題，若此問題只有正面和負面兩種答案，請設計一個 Logic circuit 直接驗證 A 先生的宣稱是否正確。

3. 
(1) (4%) A parity function over $n$ variables, $f = x_1 \oplus x_2 \oplus \cdots \oplus x_n$, has how many prime implicants?

(2) (3%) Please give the K-map of parity function over 3 variables.

4. 
(1) (6%) For the function $f(a, b, c, d) = \sum m(1, 4, 6, 7, 8, 9, 10, 11, 15)$, list all the prime implicants in a K-map and indicate which of these are essential prime implicants.

(2) (6%) Use the Quine-McClusky procedure to find all the prime implicants for $f(a, b, c, d) = \sum m(3, 7, 9, 14) + \sum d(1, 4, 6, 11)$.

(3) (5%) The prime implicants for the function

$$f(a, b, c, d, e) = \sum m(5, 7, 11, 12, 27, 29) + \sum d(14, 20, 21, 22, 23)$$

are $b'ce, ab'c, a'bec$, $b'ce$ and $acde$. Please find all the essential prime implicants and the minimal sum-of-product expression of the function.

5. 
(1) (6%) Use a PLA, as shown in following, to realize a 4-to-1 multiplexer.

(2) (5%) Implement $f(a, b, c, d) = ac' + a'b'd$ using a 4-to-1 multiplexer. Please choose the appropriate control inputs such that no extra gate was needed.
6. One wants to implement a 3-bit counter \( Q_1Q_2Q_3 \) that is reset to the 000 state and is able to count in the order of 000 \( \rightarrow \) 101 \( \rightarrow \) 111 \( \rightarrow \) 110 \( \rightarrow \) 010 \( \rightarrow \) 000 as well as in the reverse direction as shown in the following figure.

![Diagram of a 3-bit counter](image)

Design this counter with T flip-flops.

1. (6%) List the next-state tables and derive the corresponding input equations \( (T_1T_2T_3) \) for the counter to count anti-clockwise.

2. (3%) List the next-state tables and derive the corresponding input equations for the counter to count clockwise.

3. (3%) Assume an input signal UD is used to control the counting direction of the counter, and another input signal EN is used to enable and disable the counter with EN=1 and EN=0, respectively. Based on the previous results, give a logic circuit for the counter to count counter-clockwise when UD=0 and EN=1, and clockwise when UD=1 and EN=1.

4. (6%) Redo item (1) with J-K flip-flops.
7. For a mealy state machine shown as in the following table

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
<th>Output Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>X=0</td>
<td>X=1</td>
<td>X=0</td>
</tr>
<tr>
<td>S0</td>
<td>S0</td>
<td>S1</td>
</tr>
<tr>
<td>S1</td>
<td>S2</td>
<td>S0</td>
</tr>
<tr>
<td>S2</td>
<td>S0</td>
<td>S3</td>
</tr>
<tr>
<td>S3</td>
<td>S2</td>
<td>S1</td>
</tr>
</tbody>
</table>

(1) (6%) Design a synchronous circuit using D flip-flop that realizes this state table with the corresponding state assignment of S0=00, S1=01, S2=11 and S3=10. The circuit is activated at the rising-edge of the clock signal CLK.

(2) (4%) Draw a timing diagram that shows the state transition as well as the signal transition of Z by referencing to the following CLK and input X signals.

![Timing Diagram]

(3) (4%) Redesign a synchronous circuit that realizes the state table with the same state assignment using S-R flip-flops.

8. Design a circuit that realizes a filter of the form

\[ y(n) = a_1 y(n-1) + b_0 u(n) + b_1 u(n-1) + b_2 u(n-2) \]

Note that you do not need to consider the overflow problem.

(1) (4%) Assume the input \( u(n) \) and the coefficients are all 8-bit in width. Draw the data path of your circuit using an accumulator, a multiplier and other necessary multiplexers and registers. Note that you need to mark the corresponding bit-width for each data bus.

(2) (4%) Design a state machine that generates the control signals of the data-path using a state diagram.