1. (1) You have a sine-wave generator with constant resistive source impedance $R_s = 600 \Omega$, an ideal oscilloscope, a lossless probe and all kinds of variable lumped elements. Let input impedance and bandwidth of the oscilloscope be infinite, and the probe have a characteristic impedance of 100 $\Omega$ and length 30 cm. Set up an experimental procedure to measure output impedance of an amplifier at a certain frequency, say 300 MHz, using these two instruments. Formulate your setup. (8%)

(2) Shown on the left hand side at the end of this page are four types of ideal switches, namely, SPST (Single-pole single throw), SPDT (Single-pole double throw), DPST (Double-pole single throw) and DPDT (Double-pole double throw). Design a network, with two switches and conducting wires, so that the two switches can independently control whether source signal can be delivered to load or not. (5%) Design a network with three switches and each of them can independently control whether source signal can be delivered to load or not. (7%)

2. The plot shown below on the right hand side is cross section view of an enhancement PMOSFET. Let the channel region have a width of $W$ and length $L$, threshold voltage be $V_t$, the source (S) terminal be grounded, voltage at $x$ be $v(x)$, and capacitance per unit area between gate electrode and the channel be $C_{ox}$.

(1) Are source and drain heavily doped $n$- or $p$-type regions? Is its substrate of $n$- or $p$-type? Should the gate voltage be positive or negative to create a channel for current flow? (3%, given only when all answers are correct.)

(2) The voltage $v_{DS}$ produces an E-field along the channel. Give the expression of the E-field at $x$, $E(x)$, in terms of $v(x)$. (3%)

(3) Derive the $i_D$-$v_{DS}$ relationships of the transistor before and after the channel is pinched off at the drain end. Proper sign of the result should be considered. (5%, 2%)

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Circuit diagram symbols for four types of ideal switches.

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Silicon Oxide

heavily doped

heavily doped

Substrate

$S$ $v_{GS}$ $G$

$D$ $i_D$ $v_{DS}$

$B$

$x = 0$

$x = L$
3. For the MOS amplifier shown below, please answer following questions. Suppose that the MOS has parameters of $k_e=0.5mA/V^2$, $W/L=2$, $V_t=0.486V$, $C_{gs}=0.5pF$, and $C_{gd}=0.5pF$, and the Early effect of the MOS is ignored.

(a) 5% Find the $I_d$ and $g_m$ of the MOS.

(b) 6% Find the midband gain of the amplifier and upper 3-dB frequency $f_H$ by open circuit time constant method if $C_s$ is infinite.

(c) 6% Find the midband gain of the amplifier and upper 3-dB frequency $f_H$ by open circuit time constant method if $C_s$ is zero.

4. Following drawing shows a MOS amplifier, please find the $R_{in}$ (6%), $R_{out}$ (6%), and voltage gain(5%). The current source is for DC bias only. Suppose that Q1 and Q2 have small signal parameters as follows: the transconductances are $g_{m1}$ for Q1 and $g_{m2}$ for Q2 respectively, the Early resistances are infinite for both transistors.
5. The following figure shows an oscillator circuit with bias.

(1) Please derive an equation governing the circuit operation. (8%)
(2) Find the frequency of operation. (4%)
(3) Find the minimum value of the MOSFET transconductance $g_m$ for oscillations to start. (5%)

![Oscillator Circuit Diagram]

6. A matched complementary CMOS inverter has $k'_n = 50 \mu A/V^2$, $k'_p = 20 \mu A/V^2$, $V_m = -V_{pp} = 1$ V, and $V_{DD} = 5$ V. The W/L ratio of $Q_n$ is 5 μm/2 μm. The equivalent capacitance $C$ at the inverter output is 80 fF.

(1) Find the W/L ratio of $Q_p$. (3%)

(2) When the input voltage changes from 0 V to $V_{DD}$, what is the initial discharging current of the capacitance? (4%)

What is the discharging current when the output voltage goes down to $V_{DD}/2$? (4%)

(3) Find the delay-power product of the inverter. (5%)

(Assume that the switching frequency of the inverter be 1 MHz.)