共7题，满分100分，请依序答题

1. [10%] 下列叙述是否为正确，正确打 O，不正确打 X。每题二分，答错倒扣一分。
   (a) \( X + YZ = XY + XZ \)
   (b) A combinational network may have a dynamic hazard even if it is free of static hazard.
   (c) Using S-R Flip-Flop to design asynchronous networks, the networks realizing S and R must be free of 1-hazards, but S and R networks may contain 0-hazards.
   (d) It is possible to implement an asynchronous finite state machine without using any flip-flops.
   (e) A 4-bit 2's complement number system can represent integers from \(-16\) to \(15\).

2. [15%]
   (a) 設計一個 2-to-4 Decoder，有三個輸入 A、B、E (Enable Signal)以及四個輸出 D0、D1、D2、D3，寫出電路之真值表 (truth table)。 (5分)
   (b) 利用上題之 2-to-4 Decoder 當基本元件，再加上最少之邏輯閘，設計一個 3-to-8 Decoder，畫出此設計之大塊圖 (Block Diagram)，此電路有三個輸入 X、Y、Z (沒有 Enable Signal)以及八個輸出 D0、D1、D2、D3、D4、D5、D6、D7。 (5分)
   (c) 用 VHDL 描述此 3-to-8 Decoder。 (5分)

3. [11%]
   For the sequential circuit as shown:

   1% (1) Is the circuit Mealy machine or Moore machine?
6% (2) Derive and complete its state table as follows.

<table>
<thead>
<tr>
<th>q1 q2</th>
<th>q1 q2 (next state)</th>
<th>z</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>x=0</td>
<td>x=1</td>
</tr>
<tr>
<td>00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4% (3) Complete the following timing diagram assuming that delays in flip-flops and gates are zero.

4. [6%]

It is to design a sequence detector which has one input x and one output z. It gives z = 1 when x receives a consecutive sequence of 0011, and it gives z = 0 otherwise. A sample input and output sequence is shown below:

x = 001011100110011000111000101
z = 0000000000100100001000000

Derive and complete the following state transition graph for this detector if it is a Mealy machine:

- S0: reset state
- S1: one "0" received
- S2: two "0", received
- S3: two "0", one "1" received
- S4: two "0", two "1"'s received
5. [8%]
For a Mealy sequential machine with the following state table, let it have the following state assignment: \( Q_1, Q_2 = 00, 01, 11, 10 \) for states A, B, C, D, respectively. It is to implement the machine with two J-K flip flops: \( Q_1, Q_2 \).

<table>
<thead>
<tr>
<th>present state</th>
<th>next state ( x = 0 )</th>
<th>next state ( x = 1 )</th>
<th>output ( z )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>A</td>
<td>B</td>
<td>1</td>
</tr>
<tr>
<td>B</td>
<td>A</td>
<td>C</td>
<td>0</td>
</tr>
<tr>
<td>C</td>
<td>A</td>
<td>D</td>
<td>0</td>
</tr>
<tr>
<td>D</td>
<td>A</td>
<td>D</td>
<td>1</td>
</tr>
</tbody>
</table>

5% (1) Derive the input equations for \( J_1, K_1 \) of \( Q_1 \), \( J_2, K_2 \) of \( Q_2 \) and the output \( Z \), respectively.

\[
J_1 = \\
J_2 = \\
K_1 = \\
K_2 = \\
Z =
\]

3% (2) If the combinational part of the machine is to be implemented with a PLA as follows, complete the PLA with a dot indicating an AND or OR operation.
(a) Try to derive the average memory access time in terms of \( T_c \) and \( R \) of the computer system. [3%]

(b) Try to derive the average power consumption during memory access in terms of \( P_c \) and \( R \). [3%]

(c) If cache memory is to be realized by either direct-mapping or fully associative methods, try to indicate its impact on both access time \( (T_c) \) and power consumption \( (P_c) \) during memory access. [10%] Note that you should first draw block diagram of each scheme and explain how it works, and conduct performance analysis on both items.

(d) Is it always true that increasing cache size will improve both hit rate and overall memory access time? [3%]

(e) For a given multi-level For-Loop program running on the computer system, does the average memory access time remain unchanged or depend on coding style? [6%] Note that you should try to use an example to explain your solution and take page-mode of main memory into account.
7. [25%]

(a). CPU time per program is usually used to measure the speed performance for a designed processor. Give the formulation of CPU time in terms of CPI and the formulation of CPU time in terms of MIPS separately. Does the compiler affect on the value of CPI? Please discuss the issue.[5%]

(b). Given a 5-stage instruction pipeline and assumed that the Branch instruction can be resolved at the 2\textsuperscript{nd} stage, i.e., ID stage, what is the branch hazard? If the technique “delayed branch” has been used to solve the branch hazard, what is the effect on the CPI performance. Compare the performance between the techniques of “delayed branch” and “predict not-taken”. [5%]

(c). What is the meaning of the “Precise Exception” in the instruction pipelined processor? Assume an arithmetic overflow is occurred for a certain executed instruction, please describe the exception handling for this kind of exception processing.[5%]

(d). Why the displacement addressing (or called base addressing) mode is a more frequently-used addressing mode? For Load/Store instructions, please give an example of the 32-bit instruction format to show the addressing mode.[5%]

(e). Assume a processor is designed as the 5-stage pipeline with forwarding and Branch can be resolved at the 2\textsuperscript{nd} stage. For the instruction sequence shown in the following, what kinds of stalls exist in the sequence? And at which number of cycles the instruction lw in the second iteration will be fetched. Give the detail explanation.[5%]

```
Loop:  lw     $s2, 0($t1)
       sub    $s3, $s2, $s1
       add    $s4, $s4, $s3
       sw     $s4, 0($t1)
       addi   $t1, $t1, 4
       slt    $t2, $t1, Limit
       bne    $t2, $ZERO, Loop
       ....
```