A. 作業系統

1. (4%) What is degree of multiprogramming? What part of an operating systems is controlling degree of multiprogramming?

2. (9%) Write a two-process solution to the critical-section problem and prove that
   (a) Mutual exclusion is preserved: If a process is in its critical section, then the other process cannot be executing in its critical section. (4%)
   (b) The progress requirement is satisfied: If no process is in critical section and there are processes trying to enter critical sections, then eventually some process will enter critical section. (5%)

3. (12%) There is a solution to the readers-writers problem as follows.

   ```
   var mutex, wrt : semaphore;
   readcount : integer;
   
   These are the shared data structures. The semaphores mutex and wrt are initialized to 1; readcount is initialized to 0. The code for a writer process is shown as follows.
   
   wait(wrt);
   ... 
   writing is performed
   ...
   signal(wrt);
   
   The code for a reader process is shown as follows.
   
   wait(mutex);
   readcount := readcount + 1;
   if readcount = 1 then wait(wrt);
   signal(mutex);
   ... 
   reading is performed
   ...
   wait(mutex)
   readcount := readcount - 1;
   if readcount = 0 then signal(wrt);
   signal(mutex);
   
   We will develop a slightly modified algorithm which is almost the same as the above except that no more than 1000 reader processes can perform reading simultaneously. The code for a writer process remains unchanged. The code for a reader process is shown as follows (with
some unspecified statement sequence for you to answer). We need one more semaphore, named delay and initialized to 0, in the shared data structure.

```plaintext
var delay : semaphore initialized 0;
wait(mutex);
  readcount := readcount + 1;
  if readcount = 1 then begin S1 end
  else if readcount > 1000 then begin S2 end
  else begin S3 end;
  ...
  reading is performed
  ...
wait(mutex);
  readcount := readcount - 1;
  if readcount = 0 then begin S4 end
  else if readcount >= 1000 then begin S5 end
  else begin S6 end;
```

(a) Specify S1. (2%)
(b) Specify S2. (2%)
(c) Specify S3. (2%)
(d) Specify S4. (2%)
(e) Specify S5. (2%)
(f) Specify S6. (2%)

(Hint: Each statement sequence consists of zero or more statements from the set: \{signal(wrt), wait(wrt), signal(delay), wait(delay)\}.)

4. (6%) The binding of instructions and data to memory address can be done at any of the following steps: (1) compile time, (2) load time, and (3) execution time. Explain how the binding can be done at each of these steps.

5. (8%) To improve the efficiency of I/O (e.g., to improve the data transfer throughput of two application programs running on two different machines connected by a very high-speed network), several system principles can be used. For example, (1) we can reduce the number of context switches of these application programs, and (2) we can use DMA rather than programmed I/O to transmit/receive data to/from the I/O interface. List eight other useful principles.

6. (6%) Explain how to use a public key-encryption scheme to achieve data protection and person authentication.

7. (5%) List and explain five advantages of using the virtual memory (demand paging) mechanism.
B. 計算機組織

8. (5%) A base processor and two options for improving its hardware and compiler design are described as follows:

i. The base machine, \( M_{\text{base}} \):

\( M_{\text{base}} \) has a clock rate of 200 MHz and the following measures:

<table>
<thead>
<tr>
<th>Instruction class</th>
<th>CPI</th>
<th>Frequency</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>2</td>
<td>50%</td>
</tr>
<tr>
<td>B</td>
<td>3</td>
<td>20%</td>
</tr>
<tr>
<td>C</td>
<td>4</td>
<td>30%</td>
</tr>
</tbody>
</table>

ii. The machine with improved hardware, \( M_{\text{hw}} \):

\( M_{\text{hw}} \) has a clock rate of 250 MHz and the following measures:

<table>
<thead>
<tr>
<th>Instruction class</th>
<th>CPI</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1</td>
<td>50%</td>
</tr>
<tr>
<td>B</td>
<td>2</td>
<td>20%</td>
</tr>
<tr>
<td>C</td>
<td>3</td>
<td>30%</td>
</tr>
</tbody>
</table>

iii. The combination of the improved compiler and the base machine, \( M_{\text{comp}} \):

The instruction improvements from this enhanced compiler are as follows:

<table>
<thead>
<tr>
<th>Instruction class</th>
<th>Percentage of instructions executed vs. ( M_{\text{base}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>70%</td>
</tr>
<tr>
<td>B</td>
<td>80%</td>
</tr>
<tr>
<td>C</td>
<td>60%</td>
</tr>
</tbody>
</table>

(a) What is the CPI (clock cycles per instruction) for each machine?
(b) How much faster is each of \( M_{\text{hw}} \) and \( M_{\text{comp}} \) than \( M_{\text{base}} \)?

9. (a) (3%) Describe the basic concepts and advantages of Booth’s algorithm.
(b) (3%) Explain the difference between the restoring division algorithm and the non-restoring division algorithm.
(c) (2%) Calculate the largest and smallest positive normalized numbers for the IEEE 754 standard single-precision floating-point operand format.

10. (6%) Describe the following different implementations of a computer and compare their advantages and disadvantages: single-cycle, multi-cycle, and pipelined implementations.

11. (10%) It is well known that control hazard is one of the main bottlenecks during pipelining execution of instructions. You are required to describe the principles of the following two resolving methods by using simple examples clearly and briefly.

(i) What is called delayed branch technique? How to utilize the delay slot by inserting appropriate instruction instead of no-op? (5%)
(ii) How to use 2-bit branch prediction technique to reduce the branch hazard penalty? (5%)
12. (5%) What is called n-way set associative address mapping technique used in cache memory design? Give an example to explain its principle clearly. Usually, it has better hit ratio than that of direct mapping technique. Is it true? Why?

13. (10%) Compare the main differences among the following three I/O data transfer techniques: polling, interrupt, and DMA. Also describe their main advantages and disadvantages clearly and briefly.

14. (6%) Given the datapath for a multi-cycle computer and the definition and formats of its instructions,

![Datapath diagram]

FIGURE 5.32: The multicycle datapath from Figure 8.31 with the control lines shown.

- add $rd, $rs, $rt
  - #$rd = $rs + $rt
  - R-format
- lw $rt, addr($rs)
  - #$rt = Memory[$rs + addr]
  - I-format
- sw $rt, addr($rs)
  - #Memory[$rs + addr] = $rt
  - I-format
- beq $rs, $rt, addr
  - #if ($rs = $rt) go to PC + 4 + 4 x addr
  - I-format
- j addr
  - #go to 4 x addr
  - J-format

<table>
<thead>
<tr>
<th>Name</th>
<th>Fields</th>
<th>Comments</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Field size</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6 bits</td>
<td>5 bits</td>
</tr>
<tr>
<td>R-format</td>
<td>op</td>
<td>rs</td>
</tr>
<tr>
<td>I-format</td>
<td>op</td>
<td>rs</td>
</tr>
<tr>
<td>J-format</td>
<td>op</td>
<td>target address</td>
</tr>
</tbody>
</table>

(a) Write the steps taken to execute the add instruction. How many clock cycles are required for this instruction?
(b) Repeat (a) for the lw instruction.
(c) Repeat (a) for the beq instruction.