(1) [15%] True (T) or false (F). (無倒扣)

1. In RISC processors, every instruction has the same size. That is, they have the same number of bits.

2. CISC processors can provide backward compatibility with other processors in their families. This allows the CISC CPU to run the same software as used by the predecessors in its family.

3. RISC processors have fewer and simpler instructions than CISC processors.

4. Combinational logic generally has a higher propagation delay than a lookup ROM. Thus, a microcoded control unit can run at a higher clock frequency than the corresponding hardwired control unit.

5. The primary reason for including cache memory in a computer is to increase the storage of the memory system.

6. Pipeline improves throughput of the processor, but not the latency of instructions.

7. Because DMA (direct memory access) transfers data between an I/O device and the cache, it has the advantage of freeing up processor cycles.

8. ALU (arithmetic-logic unit) is a combinatorial circuit.

9. Daisy chain is a method for prioritizing multiple interrupts.

10. In virtual memory systems, a write-through policy is practical. That is, the modified information is written to both the block in the cache and to the lower level of the hierarchy.

11. In the immediate addressing mode, the instruction includes a memory address; while in the direct mode, the operand specified is not an address but the actual data to be used.

12. TLB (translation-lookaside buffer) is a cache that holds a portion of the page table.

13. Because CPI (clock cycles per instruction) depends on instruction mix, the code that executes the fewest number of instructions may not be the fastest.

14. The advantage of increasing the degree of associativity in a set-associative cache is that it usually decreases the miss rate.

15. Handshaking is a technique used for synchronous data transfers, occurring when peripherals are located within the same computer as the processor.
(2) [5%] Draw a PLA (programmable logic array) implementation of the following Boolean functions:

\[ X = AB + \overline{AB} + \overline{C} \]

\[ Y = A + \overline{B} + C \]

(3) [10%] For a computer system with a 16-bit address bus, design a 64Kx8 memory using eight 1Kx64 memory chips and any necessary additional logic circuits.

(4) [10%] Consider the following computer system with a two-level cache:

- A processor works with a base CPI (clock cycles per instruction) of 2.0, if the reference hit in the L1 cache, and a clock rate of 200 MHZ.
- The L2 has access time of 20 ns for either a hit or miss.
- A main memory has access time of 250 ns. Assume that page faults do not occur.
- The miss rate per instruction at the L1 cache is 5%.
- The miss rate per instruction at the L2 cache is 1%.

Answer the following questions:

a. [5%] If a miss occurs in the L1 cache but the miss is satisfied in the L2 cache, determine the time required for an instruction performing memory access.

b. [5%] Determine the average time required for an instruction performing memory access.
(5) [15%] Consider a multi-cycle implementation of the processor shown below.

For each of the RTL (register-transfer language) shown below

a. [5%] if (A==B) PC=ALUOut;

b. [5%] Reg[IR[15-11]]=ALUOut; #IR=Instruction register

c. [5%] MDR=Memory[ALUOut]; #MDR=Memory data register

determine the values of the following control signals:

1. PCSource  2. ALUSrcA  3. ALUSrcB  4. RegWrite  5. RegDst

Use the following notations: 1 for “activation”, 0 for “deactivation” and x for “don’t care.”
(6) [10%] Consider the following instruction:
\[ \text{lw } \$11, \$12, \$13 \ #\$11 = \text{MEM}[\$12+\$13] \]
where the corresponding machine language has the form

<table>
<thead>
<tr>
<th>OP (31-26)</th>
<th>R1 (25-21)</th>
<th>R2 (20-16)</th>
<th>R3 (15-11)</th>
<th>MISC (10-0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>38</td>
<td>12</td>
<td>13</td>
<td>11</td>
<td>0</td>
</tr>
</tbody>
</table>

Use the multi-cycle processor in problem (5) to implement the \text{lw} instruction.

a. [2%] In what cycle does the memory access \text{MEM}[\$12+\$13] actually occur?
b. [3%] Show the RTL at the 2\text{nd} cycle.
c. [2%] Show the values of ALUSrA and ALUSrB at cycle 3 (x for “don’t care”).
d. [3%] How many cycles will it take to execute this instruction?

(7) [10%] Consider a virtual memory system with the following properties:

- 32-bit virtual byte address
- 4-KB pages
- 28-bit physical byte address

The page table contains the following information:

- One valid bit
- One protection bit
- One dirty bit
- One use bit
- Physical page number

Assume that all the virtual pages are in use. Answer the following questions.

a. [3%] Decompose the 32-bit virtual address into two fields: virtual page number and page offset. Show the bit ranges of these two fields.
b. [2%] What is the number of page table entries?
c. [3%] What is the width of each entry in the page table? Show your result in bits.
d. [2%] For ease of indexing, the width of the page table is typically rounded up to a multiple of words (one word = 32 bits). What is the size of the page table? Show your result in bytes.
(8) [10%] Consider a computer system with the following characteristics:

- A memory and bus system supporting block transfer of 16 words (one word = 32 bits).
  A single block transaction consists of an address transmission followed by data.
- One clock cycle required to send an address to memory.
- A 64-bit synchronous bus clocked at 200 MHz, with each 64-bit transfer taking 1 clock cycle.
- Two idle clock cycles needed between each block transfer (bus operation). Assume the bus is idle before a memory access.
- A memory access time for every four words of 20 ns.

Assume that a bus transfer of the most recently read data and a read of the next four words can be overlapped.

a. [6%] Find the latency for a read of a 16-word block transfer.

b. [4%] Find the bus bandwidth in terms of MB/sec.

(9) [10%] The following items reflect the key ideas in pipeline. Explain these terms briefly.

a. [2%] Pipeline data hazard
b. [2%] Structural hazard
c. [2%] Branch (or control) hazard
d. [2%] Pipeline stall (or bubble)
e. [2%] Forwarding (or bypassing)

(10) [5%] A PCI bus is usually used to interface the processor and memory system. For each of the following characteristics, select the correct parameter from choices (i) and (ii).

a. [1%] Bus type: (i) I/O (ii) backplane
b. [1%] Arbitration: (i) centralized/parallel (ii) self-selection
c. [1%] Clocking: (i) synchronous (ii) asynchronous
d. [1%] Maximum bus length: (i) 0.5 m (ii) 25 m
e. [1%] Typical bandwidth: (i) 1.5 MB/sec (ii) 80 MB/sec