Part I. Multiple-choice questions (45 points total)

No partial credit will be given for the following 15 questions. Simply label the problem items (1), (2), ..., (15) and write A, B, C, or D next to each item. Each correct answer is worth 3 points, and 1 point will be deducted for each incorrect answer.

Question 1. What is $A$ for the following Boolean expression:

$$\overline{x + y}z + \overline{x}yz + (x + y)(\overline{x} + \overline{y}) = xy' + \overline{x}z + A,$$

(A) $xy'$  (B) $xz$  (C) $y\overline{z}$  (D) $xz$

Question 2. Which of the following term is not needed in the product-of-sums simplification of $\overline{x}y\overline{w} + \overline{x}zw + \overline{x}yz$, using the don't care conditions $\overline{x}y\overline{z}w + xzw + xy\overline{w}$

(A) $(\overline{x} + y)$  (B) $(\overline{y} + z)$  (C) $(z + \overline{w})$  (D) $\overline{x}$

Question 3. What is the Boolean function of the output $F$ of the following circuit.

![Circuit Diagram]

(A) $\overline{A}B + \overline{B} + C$  (B) $\overline{A} + \overline{B} + \overline{C}$  (C) $AB + \overline{C}$  (D) $ABC + \overline{B}$

Question 4. Define the carry propagate and carry generate as follows:

$P_i = A_i \oplus B_i; \quad G_i = A_iB_i$. The output carry and output sum of a full-adder become:

$C_{i+1} = C_i \oplus G_i + P_i = G_i + P_iC_i; \quad S_i = \left(P_iG_i\right) \oplus C_i$

What is the output carry $C_4$ as a function of $P_1, P_2, P_3, G_1, G_2, G_3,$ and $C_1$?

(A) $\overline{P}_3 + G_3 \overline{P}_2 + G_3 \overline{G}_2 \overline{P}_1 + G_3 \overline{G}_2 \overline{G}_1 \overline{C}_1$

(B) $P_1 + G_1 \overline{P}_2 + G_1 \overline{G}_2 \overline{P}_3 + G_1 \overline{G}_2 \overline{G}_3 \overline{C}_1$

(C) $\overline{P}_3 + G_3 \overline{P}_2 + G_3 \overline{G}_2 \overline{P}_1 + G_3 \overline{G}_2 \overline{G}_1 \overline{C}_1$

(D) $\overline{P}_1 + G_1 \overline{P}_2 + G_1 \overline{G}_2 \overline{P}_3 + G_1 \overline{G}_2 \overline{G}_3 \overline{C}_1$
Question 5. For the above circuit, which of the following is not correct?

(A) The circuit functions as a decoder
(B) A is the LSB and C is the MSB
(C) The circuit has active high output
(D) E is an enable signal and the circuit is enabled when E equals to 1

Question 6. Which of the following is not correct?

(A) the size of ROM for a BCD adder/subtractor with a control input to select between addition and subtraction is 1024x5
(B) the size of ROM for a binary multiplier that multiplies two 4-bit numbers is 256x8
(C) the size of ROM for dual 4-line to 1-line multiplexers with common selection inputs is 4096x2
(D) the size of ROM to convert a 3-bit number into an binary number that equals to the square of the input number is 8x4

Question 7. Consider a 4-input priority encoder with inputs, $D_3$, $D_2$, $D_1$, and $D_0$, and outputs, $A_1$, $A_0$, and $V$, where input $D_0$ has the highest priority and input $D_3$ has the lowest priority. Which of the following is not correct?

(A) $V = D_0 + D_1 + D_2 + D_3$
(B) $A_0 = D_1 + D_0 \overline{D_2}$
(C) $A_1 = \overline{D_0} \overline{D_1}$
(D) there is no don’t care condition when $D_2 = 1$ for all outputs
**Question 8.** Consider the sequential circuit design of a $T$ flip-flop using a $D$ flip-flop. Which of the following logic gate is needed in the circuit?

(A) AND  
(B) OR  
(C) NOT  
(D) Exclusive-OR

**Question 9.** What is the main problem associated with clock gating?

(A) using more gates  
(B) consuming more power  
(C) causing clock skew  
(D) none of the above

**Question 10.** Consider the following master-slave flip-flops. Which of them can in fact be regarded as edge-trigged?

<table>
<thead>
<tr>
<th>Flip-Flop</th>
<th>Master</th>
<th>Slave</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>$D$ latch</td>
<td>$D$ latch</td>
</tr>
<tr>
<td>B</td>
<td>$D$ latch</td>
<td>$SR$ latch</td>
</tr>
<tr>
<td>C</td>
<td>$SR$ latch</td>
<td>$D$ latch</td>
</tr>
<tr>
<td>D</td>
<td>$SR$ latch</td>
<td>$SR$ latch</td>
</tr>
</tbody>
</table>

(A) only A  
(B) A and B  
(C) only C  
(D) C and D

**Question 11.** Consider a sequence recognizer which is to recognize the occurrence of bits 0010 on input $X$ by making output $Z$ equal to 1 only when the previous three inputs to the circuit were 001 and current input is a 0. What is the minimum number of states required for the circuit?

(A) 1  
(B) 2  
(C) 3  
(D) 4

**Question 12.** A switching-tail ring counter is a shift register which uses the complement of the serial output as the serial input. Starting from an initial state of 0101, how many clock pulses will move the counter to the state of 1101?

(A) 5  
(B) 6  
(C) 7  
(D) 8
Question 13.

Consider the 4-bit synchronous counter shown above. Which of the following state changes will require the longest time for the outputs to change?

(A) 1110 → 1111  (B) 1111 → 0000  (C) 0000 → 0001  (D) none of the above

Question 14. Inputs $X_i$ and $Y_i$ of each full adder in an arithmetic circuit have digital logic specified by the Boolean functions

$$X_i = A_i, \quad Y_i = \overline{S} C_{in} B_i + S C_{in} + S C_{in} \overline{B_i}$$

What is the arithmetic operation for $S = 1$ and $C_{in} = 0$?

(A) $A + 1$  (B) $A - 1$  (C) $A + B$  (D) $A - B$

Question 15. A data path has five major components, $A$ through $E$, attached in a loop. The maximum delay of each of the components is $A$, 2 ns; $B$, 1 ns; $C$, 3 ns; $D$, 4 ns; and $E$, 3 ns. What is the maximum clock frequency that can be used for the datapath if the datapath is pipelined using three stages?

(A) 76.9 MHz  (B) 166.7 MHz  (C) 200 MHz  (D) 250 MHz
Part II (9 points total)

(i) (4pts) Implement the following Boolean function as closed paths through an n-channel switch model network using a minimum number of transistors. Draw the circuit diagram.

\[ F(X, Y, Z) = YZ + \overline{X}Z + XY \overline{Z}. \]

(ii) (5pts) Implement the following circuit using 2 inverters and 2 transmission gates. Draw the circuit diagram.

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>High-Imp.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Part III (8 points total)  Design a BCD-to-excess-3 code converter using PLA. List the programming table and draw logic diagram.

Part IV (12 points total)  Consider the circuit that accepts a 4-bit number, \( A_3, A_2, A_1, \) and \( A_0, \) and generates a 3-bit number, \( S_2, S_1, \) and \( S_0, \) that is the result of performing mod-5 operation on the input number.

(i) (8 pts) Design the circuit using 8x1 multiplexers.

(ii) (4 pts) Design the circuit using decoder
Part V (12 points total)

(i) (8 pts) Use $D$ flip-flops ($S_2, S_1, \text{ and } S_0$) to design a counter with the following repeated binary sequence: $0, 1, 2, 3, 4, 5$.

(ii) (4 pts) Give the count sequence for an initial count equal to 6.

Part VI (6 points total)

Three register transfer statements are given. Otherwise, AR is unchanged.

$$C_A: AR \leftarrow AR + 1$$

$$\overline{C_A}C_B: AR \leftarrow AR + BR$$

$$\overline{C_A} \overline{C_B}: AR \leftarrow BR$$

Using a 4-bit counter with parallel load, a 4-bit adder, and external gates, draw the logic diagram that implements these register transfers.

Part VII (8 points total)

Design a sequential circuit for the state diagram given below. Use $JK$ flip-flop for the higher order state variable, $S_1$, and $T$ flip-flop for the lower order state variable, $S_0$.

![State Diagram](image)