1. The source follower in Fig. 1 has a saturated load. The transistor parameters are $V_t$(threshold voltage) = 1V, and $k=2\text{mA}/V^2$ for transistor Q1 and $V_t=1V$ and $k=0.2\text{mA}/V^2$ for transistor Q2.

Assume that the channel length modulation factor $\lambda=0$ for both transistors and $V_{DS}=9V$.

(a) (4%) Determine $V_{GG}$ such that the quiescent value of $V_{DS}$ of Q2 is 4V

(b) (4%) Assume $R_L=\infty$, please derive the small signal voltage gain.

(c) (6%) Please calculate the small signal voltage gain for $R_L=10k\Omega$

(d) (4%) Please determine the output resistance $R_o$.

The current equations in nMOSFET are in the following:

$I_D(\text{triode})=k((V_{GS}-V_t)V_{DS}-0.5V_{DS}^2)$

$I_D(\text{saturation})=0.5k(V_{GS}-V_t)^2$

2. Consider the current mirror shown below, in which $I_a=1\text{mA}$ is an ideal current source. The BJTs, Q1 and Q2, are identical, and have the following I-V characteristics in the forward-active region:

$I_C = I_S e^{V_{BE}/V_T} \times \left(1 + \frac{V_{CE}}{V_A}\right)$

$I_B = \frac{I_S}{\beta_F} e^{V_{BE}/V_T}$

where $I_S$ is the saturation current, $V_T = kT/q$ is the thermal voltage, $V_A$ is the Early voltage, and $\beta_F$ is the forward current gain. Assume $V_{BE(on)} = 0.8V$ and $V_A = 2V$.

a. [6%] Find $I_O$ if $\beta_F = 20$, and $V_A = \infty$.

b. [8%] Find $I_O$ if $\beta_F = 20$, and $V_A = 10V$. 

![Current Mirror Diagram](image_url)
3. Consider the transimpedance amplifier shown below, where $I_s$ is the current input and $V_o$ is the voltage output. Assume all transistors are biased in the forward-active region. Let $g_m = g_{m2} = g_{m1} = 4 \, \text{mA/V}$. Assume $r_o = \infty$ for all transistors, and consider only $C_s$ and $C_1$ for capacitive effects.

a. [6%] Let $R_2 = 1\, \text{k}\Omega$, calculate the dc loop gain $A\beta$ of this feedback circuit.

b. [6%] Let $C_1 = 0$ and $R_2$ is adjusted so that the dc loop gain $A\beta = 50$, what is the $-3\, \text{dB}$ bandwidth of this transimpedance amplifier?

c. [7%] Let $R_2$ be adjusted so that the dc loop gain $A\beta = 50$, what is the maximum value of $C_1$ to achieve at least $45^\circ$ phase margin for the feedback loop? Hint: $C_1 < C_s$.

4. The following is a push-pull power amplifier. The input signal has a triangular waveform as shown below. The load $R_L$ is $5\, \text{Ω}$. The average power dissipated in the load is $10\, \text{W}$.

a (5%) What is the minimum value of the supply voltage, $(Vcc)\text{min}$?

b (5%) When $Vcc=(Vcc)\text{min}$, what is the average power dissipation in transistors Q1 and Q2?

c (5%) When $Vcc=(Vcc)\text{min}+5\, \text{V}$, what is the average power dissipation in Q1 and Q2.
5. A CMOS astable circuit is shown in the following. Clamping diodes are connected at the input terminals to prevent the input signal from rising above $V_{DD} + V_D$ and falling below $-V_D$ ($V_D$ is the diode voltage drop). Assume $R_{ON} << R$ and $V_{ao} = -0.5V_{DD}$ where $R_{ON}$ and $V_{ao}$ are the output resistance and the threshold voltage of the CMOS gates respectively.

a. (6%) For $V_D = 0V$ (Clamping diodes are assumed ideal), sketch the waveforms of $V_i$, $V_o$, and $V_{ao}$, and derive the period $T$. Is the period $T$ a function of $V_{DD}$?

b. (6%) Repeat (a), but now for $V_D = 0.5V$, is the period $T$ a function of $V_{DD}$?

![CMOS astable circuit diagram]

6. A circuit of a NAND gate is shown below. Inputs A and B are connected. Assume $\beta_F = 30$, $\beta_R = 0.1$, $V_{BE\text{Sat}} = 0.8V$, $V_{CE\text{Sat}} = 0.2V$ and neglect leakage currents.

a. (5%) For $V_i = 0V$, find numerical values for $I_{B1}$, $I_{B2}$, $I_{B3}$, and $V_o$.

b. (3%) Estimate a numerical value for $V_i$ when $V_o$ switches to logic zero.

c. (14%) For $V_i = 4.5V$ and use $V_{BC1} = 0.6V$, find numerical values for $I_{B1}$, $I_{B2}$, $I_{C2}$, $I_{B3}$, $I_{C3}$ and $V_o$ and determine the region of operation for Q1, Q2, and Q3.

![NAND gate circuit diagram]