The following equations are for drain current in a nMOSFET. They may be useful in your answering the following questions.

\[
I_D(\text{triode}) = k_n(W/L)n (V_{GS}-V_{th})V_{DS} - 0.5V_{DS}^2
\]
\[
I_D(\text{saturation}) = 0.5k_n(W/L)n (V_{GS}-V_{th})^2(1 + \lambda V_{DS})
\]

where \( k_n = \mu_n C_{ox} \). \( V_{th} \) is threshold voltage. The subscript \( n \) denotes a n-type MOSFET.
\( \lambda = 1/V_A \) is the channel length modulation factor.

1. In the following circuit (Fig. 1), Q2=Q3 (matched), \( V_{th} \) (threshold voltage) = \( V_{pp} = 1V \);
\( \mu_n C_{ox} = 2 \mu_p C_{ox} = 20 \mu A/V^2 \), \( (W/L)_n = 100/1 \); \( V_{th} \) (Early voltage) = \( V_{pp} = 40V \).
Neglect the Early effect for DC analysis and when evaluating the transconductance \( g_m \).

(a) Find \( R \) to obtain \( I_R = 200 \mu A \). (3%)
(b) For the circuit to have maximum small signal voltage gain, find the DC bias \( V_I \), the DC output current \( I_{D1} \), the mode of operation of Q1 and Q2, and the small-signal voltage gain of this amplifier. (9%)
(c) If the DC bias \( V_I = 2V \), find the DC output current \( I_{D1} \), the DC output voltage \( V_o \), the Q1 and Q2 operation mode. (3%)

\[ \text{Fig. 1} \]

2. In the following TTL gate (Fig. 2), assume all transistors are identical. \( V_{BE(\text{active})} = 0.7V \), \( V_{BE(\text{saturation})} = 0.8V \), \( V_{CE(\text{saturation})} = 0.1V \), \( \beta_f = 100 \), \( \beta_R = 0.1 \). fan-out = 1.

(a) Specify which region (forward-active, reverse-active, off, saturation) each transistor is in when \( V_{in} \) is logic "1". (4%)
(b) Specify which region each transistor is in when \( V_{in} \) is logic "0" (4%)
(c) At the instant when \( V_{in} \) switches from "1" to "0", specify which region the transistor Q1 and Q6 are in. (2%)
(d) If Q6 is removed (i.e., R2 and R5 connected to ground directly), sketch \( V_o \) versus \( V_{in} \) and specify the voltages at the breakpoints. (6%)

\[ \text{Fig. 2} \]
(3) The following four circuits have errors. Please briefly point out the error in each circuit and redraw the correct circuit. (12%)

(a) BJT Current Mirror

(b) BJT CE-CB Cascade Amplifier

(c) BJT Differential Amplifier

(d) BJT CE Amplifier

(4) Assuming the Op-Amp is ideal in the circuits in Fig. 4(a) and 4(b) with +5V and -5V output saturation levels.

(a) Sketch and level the transfer characteristic of v₀ versus v₁ for each circuit. (9%)
(b) For a 100mV-amplitude sine-wave input having zero average, what will be the waveform of v₀₁ and v₀₂, respectively. (6%)
(5) In Fig. 5, the Op-Amp is ideal but with the input offset voltage $V_{os}$. The power supply voltages of the Op-Amp are +5V and -5V.

(a) Assume that $V_1=0.5V$, $V_2=1V$ and $V_{os}=0V$. If the switch S is closed, calculate $V_o$. (4%)
(b) The same as in (a) but with the switch S open and negligible switch transients, calculate $V_o$. (4%)
(c) The same as in (a) but with $V_{os}=+5mV$, calculate $V_o$. (4%)

(6) The following circuit (Fig. 6) shows a feedback amplifier,

(a) Identify the feedback topology of the above amplifier. Calculate the feedback factor $\beta$. (7%)
(b) Identify the feedback type, positive or negative feedback? why? (3%)
(c) Replace the NMOS device Q3 by a pMOS device and keep all other circuits unchanged. Draw the PMOS Q3 amplifier stage. Identify the feedback type. (5%)

(7) In the following CMOS inverters, assume the k and W/L of all nMOSFETs and pMOSFETs are the same. $V_{th}=0.8V$ and $V_{tp}=-0.8V$. $\lambda=0$

(a) Determine the range of $V_{o1}$ for which N1 and P1 are biased in the saturation region. (5%)
(b) If $V_{o2}=0.6V$, determine the values of $V_{o3}$, $V_{o1}$ and $V_I$. (10%)