1) Find the output voltage $V_o$ in the circuit of the non-ideal op amp with input resistance of $1 \text{M}\Omega$, gain of 20, and output resistance of $1 \text{K}\Omega$. (10%)

2) For the circuit shown below, assume that the OP-amp is ideal and the charge stored on the capacitance $C_1$ is zero at $t = 0$ sec. For $t > 0$ sec., what is the output voltage $V_o(t)$? (10%)
3) An OP AMP is used in the circuit of 4-bit digital/analogue converter (DAC) shown below. D₃ ~ D₀ are digital signals with logic ‘1’ of 5V and logic ‘0’ of 0V. Please find the resistance R₁ ~ R₈ to make the output analogue voltage Vₒ to be:

\[ Vₒ = -(1/3) \left[ D₃ \times 2^3 + D₂ \times 2^2 + D₁ \times 2^1 + D₀ \times 2^0 \right] V \]  

(16%) 

4) Assuming Q₁ and Q₂ are equal: \( Vᵢ = 2V \), \( \muₜCox = 20\mu A/V^2 \), \( L = 10\mu m \), \( W = 100\mu m \), \( \lambda = 0 \), find \( V_D₁ \), \( V_D₂ \), \( I_D₂ \).  

(15%)
5) Consider the source-follower circuit below with transistor parameters $V_{TN} = 1.2\,\text{V}$, $K_n = 0.5\mu\text{nA}/\text{V}^2$, and $\lambda = 0.01\,\text{V}^{-1}$. If $I_Q = 1\,\text{mA}$, determine the transconductance, the small-signal voltage gain $A_v = \frac{v_o}{v_i}$ and the output resistance $R_o$. \hfill (15\%) \\

6) Consider an active-loaded common-emitter amplifier. Let the amplifier be fed with an ideal voltage source $V_i$ and neglect the effect of $r_s$. Assume that the bias current source has a very high resistance and that there is a capacitance $C_L$ present between the output node and ground. This capacitance represents the sum of the input capacitance of the subsequent stage and the inevitable parasitic capacitance between collector and ground. Draw the small signal circuit and show that, for small $C_{\mu}$ the voltage gain is given by $\frac{V_o}{V_i} = -\frac{g_m r_o}{1 + s(C_L + C_{\mu}) r_o}$. \hfill (10\%)
7) A class AB output stage using a two-diode bias network as shown below utilizes diodes having the same junction area as the output transistors. For $V_{cc} = 10 \, \text{V}$, $I_{BIAS} = 0.5 \, \text{mA}$, $R_L = 100 \, \Omega$, $\beta_N = 100$, and $|V_{CEsat}| = 0 \, \text{V}$, what is the quiescent current? What are the largest possible positive and negative output signal levels? To achieve a positive peak output level equal to the negative peak level, what value of $\beta_N$ is needed if $I_{BIAS}$ is not changed? (12\%)

8) The differential amplifier shown below utilizes a resistor $R_{ss}$ to establish a 1-mA dc bias current. Note that this amplifier uses a single 5-V supply and thus needs a dc common-mode voltage $V_{CM}$. Transistors $Q_1$ and $Q_2$ have $k_n (W/L)_n = 4 \, \text{mA/V}^2$, $V_t = 0.7 \, \text{V}$, and $\lambda = 0$. (12\%)

(a) Find the required value of $V_{CM}$.
(b) Find the value of $R_D$ that results in a differential gain $A_d$ of 10 V/V.
(c) Determine the dc voltage at the drains.
(d) Determine the common-mode gain $\Delta V_{D1}/\Delta V_{CM}$.