(1) For the circuit shown below, assume the operational amplifiers are ideal.

![Operational Amplifier Circuit](image)

(a) Find and plot the transfer characteristic $V_{o1}$ as a function of $V_i$, (8%)
(b) Find and plot the transfer characteristic $V_o$ as a function of $V_i$, (8%)

(2) Consider the differential amplifier shown below. Let $(W/L)_{M3} : (W/L)_{M6} = 1:4$. Assume all the devices are operated in saturation region, and $R_L$ is much greater than $r_o$.

![Differential Amplifier Circuit](image)

(a) If M1 and M2, M3 and M4 are perfectly matched, $r_{o1} = r_{o2} = r_{o3} = r_{o4} = r_{o5} = 100k \Omega$, $g_{m1} = g_{m2} = g_{m3} = g_{m4} = 1$ mA/V. Derive the small signal differential mode voltage gain $A_{dm}$ and common mode voltage gain $A_{cm}$, (12%)
(b) If $(W/L)_{M1} : (W/L)_{M2} = 100 : 99$, $(W/L)_{M3} : (W/L)_{M4} = 99 : 100$, $\mu_n C_{ox} (W/L)_{M1} = 0.1$ mA/V, and $\mu_n C_{ox} (W/L)_{M2} = 0.099$ mA/V. Neglect channel length modulation effect ($r_o$), find the input offset voltage. (4%)

(3) A pass-transistor logic circuit is shown below.

![Pass-Transistor Logic Circuit](image)

(a) Determine the truth table for this circuit. What logic function does it implement? (8%)
(b) In this circuit, the p-MOSFET Mp is a weak pull-high device. Assume the input signal at nodes A or B has a voltage level of 5V for logic “1", and a voltage level of 0V for logic “0”, $\mu_n = 3 \mu_p$, and the threshold voltage $V_{tp} = V_{tn} = 0.6V$. Without considering the fan-out effect at the node Y, how to design the ratio of $[ (W/L)n / (W/L)p ]$ to get a voltage level of logic “0” below 0.5V at the output node Y? (8%)
(4) In the following CMOS circuits, the current equation in the nMOSFET is as follows:

\[
\begin{align*}
I_D &= k (V_{GS} - V_T)^2 \\
I_D &= k (2(V_{GS} - V_T)V_{DS} - V_T)^2
\end{align*}
\]

(saturation region) 
(triode region)

where \( k = 0.5 \mu C_{ox}(W/L) \) and \( V_T \) is the threshold voltage of the nMOSFET. The current equation in the pMOSFET can be derived likewise. \( V_{DD} = 5V \), \( k(nMOS) = 2mA/V^2 \), \( k(pMOS) = 0.5mA/V^2 \), \( V_i(nMOS) = 0.6V \), \( V_i(pMOS) = -0.8V \).

(a) For a CMOS inverter (Fig. (a)), the \( V_O \) versus \( V_I \) is shown in Fig. (b). Please calculate the values of \( V_1, V_2, V_3, V_4 \). (8%)

(b) In a CMOS amplifier (Fig. (c)), what is the value of \( V_{GG} \) that the small-signal voltage gain \( A_v = V_o/V_i \) has a largest value? For \( R_i = 10k\Omega \), \( C = \infty \), what is the maximum small-signal voltage gain? (8%)

(5) Consider the feedback amplifier shown below. Assume all the MOSFETs are operated in saturation region. \( g_{m1} = g_{m2} = 1 \text{ mA/V}^2 \).

(a) If the output voltage is taken at \( V_{o1} \), which feedback type is adopted in the circuit (shunt-shunt, shunt-series, series-shunt, series-series). (3%)

(b) If the output voltage is taken at \( V_{o2} \), which feedback type is adopted in the circuit (shunt-shunt, shunt-series, series-shunt, series-series). (3%)

(c) Find the low frequency small signal gain of \( V_o/I_i \). (7%)

(d) If \( C_p = 1 \text{ nF} \) and neglect all the other parasitic capacitances. Find the -3 dB bandwidth of \( V_{o2}/I_s \). (7%)
(6) Consider the class B output stage, as shown below. Assume the devices have $|V_d|=1\text{V}$, $\mu C_{ox}(W/L)=200\text{mA/V}^2$, and the load resistance is very high, i.e., $R_{L}\to\infty$:

![Diagram of class B output stage]

(a) Plot the transfer curve $v_o$ versus $v_i$ and indicate the input voltage range and the output voltage range. (8%)

(b) When a bias voltage $V_{GG}$ is applied between the gates of the two MOSFETs, the circuit becomes a class AB output stage. What value of $V_{GG}$ is required to reduce the incremental output resistance $R_o$ in the quiescent state to $10\Omega$? (8%)