共五題，請依序答題

1. [10%]
評估 CPU 的運算速度，常見到 MIPS, MOPS, CPI 值表示。請問它們分別代表何種意義？MIPS 與 MOPS 彼此之間有何關係？MIPS 與 CPI 彼此之間有何關係？

2. [20%]
RISC Processor 指令執行，常分五步驟進行，即
Instruction_Fetch (IF)
Decode and Register_Fetch (RF)
Execution (EX)
Memory_Access (MEM)
Register_Write_Back (WB)
(1) 何謂 Memory_Access？何謂 Register_Write_Back？[5%]
(2) 五步驟執行指令，有三種時間規格
      (I) 五步驟加起來的時間，以一個 clock cycle 完成
      (II) 每步驟各以一個 clock cycle 完成，但沒有 pipelining
請問(I) 與(II) 那種 Processor 速度快？
請問(I) 與(II) 那種 Processor 硬體較省？[5%]
(3) 根據五步驟執行指令，請畫出 data path 的硬體架構，使得它可執行 Load, Store, Add 指令。[5%]
(4) 何謂 base addressing（也稱 displacement addressing）？
    為何它常被用作 memory access？[5%]

3. [20%]
無題的五步驟常以 pipelining 方式執行指令，使得速度可以加快，但會有 hazard 發生，可能使得速度降低。
(1) 何謂 data hazard？請舉一例說明。[5%]
(2) 何謂 control hazard？請舉一例說明。[5%]
(3) Hazard 可用 software 或 hardware 方式消除，請各舉一例說明。[5%]
(4) 何謂 dynamic pipeline scheduling？何謂 superscalar processor？二者有何關係？[5%]
4. [20%]
In the following, you’re asked to design an Arithmetic Logic Unit (ALU) needed in a CPU. This ALU contains the following five operations: ADD, EXOR, EXNOR, AND, OR.

(1) Draw the truth table for an ALU containing these five operations. [4%]
(2) Design the ALU using the Multiplexer (MUX) to implement these five operations. [8%]
(3) Design the ALU using the Multiplexer (MUX) to implement these five operations. [8%]

5. [30%]
Memory hierarchy is the concept of using memory in a computer system to improve system performance, where the main memory is used to store frequently accessed data, while secondary memory is used to store less frequently accessed data. [4%]

(1) In a computer system, the memory hierarchy is used to store frequently accessed data, while secondary memory is used to store less frequently accessed data. [4%]
(2) What is "Harvard Architecture"? Please explain how it works. [8%]
(3) A computer with a Harvard Architecture uses two different memory spaces: one for program instructions and another for data. [8%]
// Pseudo C-code segments:

```c
for (i=0; i<N; i+2)
    for (j=0; j<N; j+2)
        Y = (X[i][j] + X[i][j+1] + X[i+1][j] + X[i+1][j+1]) / 4;
```

where the cache memory size is N and the CPU has the following features:

- If 4 X's are available at register files, it takes 2 time units (2T) to compute one "Y";

- It takes 1 time unit (1T) to load 2 X’s from cache memory to register files;

- It takes 5 time units (5T) to load 2 X’s from main memory to register files;

- Data loads of the following types can be done simultaneously: (a) between main memory and cache memory, (b) between cache memory and register files

(4) 若上述的 C-codes 削由一組相同的 CPU (例如 4 個 CPU's) 來執行。此 CPU's 的特性如上所述，同時共用相同的主記憶體 (main memory)。若考慮到可能的記憶體使用方式，來確保執行 C-codes 所花的運算時間是最少的 (in terms of time unit T)。 (Note that you can first make an assumption of a target multi-processor architecture and then schedule operations to the allocated CPU’s.) [10%]