A. Please answer the following questions briefly.

(1) (a) Explain why a bipolar junction transistor (BJT) usually has larger current driving capability than a MOSFET in VLSI circuits.
(b) In a BJT amplifier, why is the emitter-base capacitance \(C_e\) usually larger than the collector-base capacitance \(C_b\)?
(c) What is the advantage of a CMOS transmission gate over a nMOS transmission gate with respect to the output voltage level? (8%)

(2) In the following two nMOSFET current sources, all the nMOSFETs have matched device parameters. But the channel width of M2 and M4 is 2 times that of M1 and M3. \(V_{GS1}=V_{GS3}=1\text{V}, V_{DS1}=2\text{V}\). (6%)
(a) If the equivalent Early voltage \(1/\lambda = \infty\) (where \(\lambda\) is the channel length modulation factor), calculate \(I_{outA}\) and \(I_{outB}\).
(b) If the equivalent Early voltage \(1/\lambda = 30\text{V}\), calculate \(I_{outA}\) and \(I_{outB}\).

3. In the BJT differential amplifier, \(r_o\) is the output resistance of the current source I. Q1 and Q2 are perfectly matched. (6%)
(a) If \(r_o\) is increased, what are the changes of the mid-band differential mode gain \(A_{dm}\) and the mid-band common mode gain \(A_{cm}\)?
(b) Repeat (a) for \(R_E\).
(c) Describe (without calculation) the effect of \(C_e\) on the differential mode gain \(A_d(s)\) and the common-mode gain \(A_e(s)\).
A variable-shift clamping circuit is shown as follows. The input voltage $v_i(t) = 10\sin(\omega t)$ volts is applied at $t=0$. Draw the waveform of the output voltage $v_o(t)$ during the first two cycles of the input voltage ($0 < \omega t < 4\pi$). You need to specify the values of $v_o$ at $\omega t = 0.5\pi, \pi, 1.5\pi, 2\pi, 2.5\pi, 4\pi$ in your plot. Assume that the diode is ideal and $C = \infty$. (8%) 

5. Please sketch the $I-V$ curve of the following circuit. (3%) 

6. For the CMOS logic gate below, please complete the PMOS network with minimal transistors. (3%) 

B. Computational Problems 

7. For the circuit shown below, assume $R_e = 2K\Omega, R_c = 1K\Omega, R_l = 2K\Omega, R_t = 10K\Omega, C_e = C_c = \infty$. For transistor Q1, $\beta = \infty$, $V_{CE, sat} = 0V$ and $V_{T, active} = 0.7V$. (10%)
8. In the following circuit, assume $R_i=6\,\text{k}\Omega$, $R_2=3\,\text{k}\Omega$, $R_c=3.3\,\text{k}\Omega$, $R_e=2\,\text{k}\Omega$, $R_L=330\,\text{\Omega}$, $C_{\text{c}}=C_{\text{e}}=C_{\text{c}}=\infty$. For transistor Q1, the base spread resistance $r_B=20\,\Omega$, $r_e=150\,\Omega$, $r_o=\infty$, $C_{\text{e}}=10\,\text{pF}$ and $g_{m}=500\,\text{mA/V}$.

(a) If $V_C=6\,\text{V}$, find the peak-to-peak value of the maximum symmetrical collector current swing.
(b) Find the value of $R_2$ that will produce the largest symmetrical collector current swing. What is the peak-to-peak value of the maximum symmetrical collector voltage swing?

9. The voltage transfer curve of an inverter is shown in Fig. (a), which is assumed to be piecewise linear. In Fig. (b), two inverters (inverter 1 and inverter 2) are connected as a buffer. The voltage transfer curve of the buffer is shown in Fig. (c). The inverter 1 has $\text{Vol}_1$, $\text{Voh}_1$, $\text{Vil}_1$ and $\text{Vih}_1$ and the inverter 2 has $\text{Vol}_2$, $\text{Voh}_2$, $\text{Vil}_2$ and $\text{Vih}_2$. (10%)

(a) Find the midband current gain, $A_{\text{in}}=i_i/i_i$.
(b) If $C_{\text{e}}=0.1\,\text{pF}$, find the upper 3dB frequency of $A_{\text{in}}$.

10. In the following amplifier, the transconductance $g_{m}(\text{M5})$ of M5 is 0.5mA/V. The current sources $I_1$ and $I_2$ have infinite output resistance. (15%)

(a) What is the necessary and sufficient condition to have $\text{Vil}_B=\text{Vil}_1$, $\text{Vih}_B=\text{Vih}_1$, $\text{Vol}_B=\text{Vol}_2$, $\text{Voh}_B=\text{Voh}_2$?
(b) If $\text{Vol}_1=1\,\text{V}$, $\text{Voh}_1=\text{Voh}_2=4\,\text{V}$, $\text{Vil}_1=\text{Vil}_2=2\,\text{V}$, $\text{Vih}_1=\text{Vih}_2=3\,\text{V}$, what are the values of $\text{Vol}_B$, $\text{Voh}_B$, $\text{Vil}_B$, $\text{Vih}_B$?
11. Design a DC millivoltmeter circuit of the form shown below. The full-scale deflection current of the moving coil is IM(max) = 100μA and the full scale reading will be VS(max) = 100mV with IS(max) = 1μA. All the resistors should be in the range from 1kΩ to 100kΩ. Assume that the Op-Amp has Rf = ∞ and AV = ∞. Explain why the value of R3 you have selected. (8%)

![Circuit Diagram](image)

12. The following figure shows a MOS double cascode amplifier with active load. Find the low-frequency small-signal voltage gain AV = VO/V1. Use the transconductance of Q1, Q2 and Q3 (gm1, gm2, gm3) and the output resistance (ro1, ro2 and ro3) in your result. (5%)

![Circuit Diagram](image)

13. In the following circuit, the Op-Amp is ideal. R2 = 100kΩ, R3 = 5kΩ, R4 = 50kΩ. The voltage across the Zener diode in forward bias is 0.5V and the Zener breakdown voltage is 5V. (10%)

![Circuit Diagram](image)

(a) If R1 = 20kΩ, what is the small-signal voltage gain VO/V1?
(b) If R1 = 5kΩ, please draw the characteristics of VO versus V1. Specify the values at the breakpoints.