1. (a) (5%) The producer process and the consumer process share a bounded buffer and use the following algorithm to synchronize their operations. Determine the maximum number of buffers that can be full at the same time.

```pascal
var n;
type item = ...;
var buffer: array [0..n-1] of item;
in, out: 0..n-1;
in := 1;
out := 0;

producer process:
repeat
  ...
  produce an item in nextp
  ...
  while in+1 mod n = out do no-op;
  buffer[in] := nextp;
in := in+1 mod n;
until false;

consumer process:
repeat
  while (out+1) mod n = in do no-op;
  out := out+1 mod n;
  nextc := buffer[out];
  ...
  consume the item in nextc
  ...
until false;
```

(b) (10%) Can the following algorithm be used to synchronize producer-consumer operations? (ii) If your answer is yes, give your reasons. Otherwise, explain the problems and modify the algorithm to make it right.

```pascal
producer process:
repeat
  ...
  produce an item in nextp
  ...
  while counter = 0 do no-op;
  buffer[in] := nextp;
in := in+1 mod n;
  counter := counter + 1;
until false;

consumer process:
repeat
  while counter = 0 do no-op;
  nextc := buffer[out];
  out := out+1 mod n;
  counter := counter - 1;
  ...
  consume the item in nextc
  ...
until false;
```

2. (5%) The disk allocation methods allocate disk space to files so that disk space is utilized effectively and files can be accessed quickly. How does UNIX allocate data blocks of a file on a disk? Draw a figure to show its structure.

3. (5%) Is it true that, for FIFO page-replace algorithm, the page-fault rate may increase as the number allocated frames increases? Explain briefly.

4. (10%) Consider the following set of processes, with the length of the CPU burst time given in milliseconds:
<table>
<thead>
<tr>
<th>Process</th>
<th>Arrival time</th>
<th>Burst time</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>0</td>
<td>60</td>
<td>1</td>
</tr>
<tr>
<td>P2</td>
<td>10</td>
<td>40</td>
<td>2</td>
</tr>
<tr>
<td>P3</td>
<td>30</td>
<td>25</td>
<td>3</td>
</tr>
<tr>
<td>P4</td>
<td>50</td>
<td>10</td>
<td>2</td>
</tr>
<tr>
<td>P5</td>
<td>70</td>
<td>15</td>
<td>3</td>
</tr>
</tbody>
</table>

Draw the Gantt charts illustrating the execution of these processes and compute the turnaround time of each process, using the following scheduling algorithms:
(a) A nonpreemptive priority scheduling, a smaller priority number implies a lower priority.
(b) A Round-robin scheduling, with quantum = 10.

5. (10%) Consider the following snapshot of a system for deadlock avoidance of resource allocation, with 4 types of resources, A,B,C,D:

<table>
<thead>
<tr>
<th>Process</th>
<th>Allocation</th>
<th>Max</th>
<th>Available</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A B C D</td>
<td>A B C D</td>
<td>A B C D</td>
</tr>
<tr>
<td>P0</td>
<td>0 1 0 2</td>
<td>4 1 2 2</td>
<td>2 1 1 2</td>
</tr>
<tr>
<td>P1</td>
<td>2 1 1 0</td>
<td>2 1 3 3</td>
<td></td>
</tr>
<tr>
<td>P2</td>
<td>1 0 1 1</td>
<td>1 2 1 2</td>
<td></td>
</tr>
<tr>
<td>P3</td>
<td>0 2 2 0</td>
<td>3 2 2 3</td>
<td></td>
</tr>
</tbody>
</table>

(a) Show that the system is in a safe state.
(b) If a request from process P3 arrives for (1,0,0,1), show whether the request can be granted immediately.

6. (5%) How does a system call work?

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7. (a) (2%) Define the term “Instruction Set Architecture.”
(b) (6%) State the characteristics of the following instruction set styles: i. accumulator, ii. memory-memory, iii. stack, and iv. load-store (register-register).

8. Suppose we enhance a machine making all floating-point instructions run five times faster.
(a) (3%) If the execution time of some benchmark before the floating-point enhancement is 20 seconds, what the speedup will be if one-fourth of the 20 seconds is spent executing floating-point instructions?
(b) (4%) If the execution time of a benchmark before the floating-point enhancement were 100 seconds, how much of the initial execution time would floating-point instructions have to account for to show an overall speedup of 2 on this benchmark?
9. (4%) Fill in the following table to determine Booth's algorithm in terms of the bit values of the multiplier:

<table>
<thead>
<tr>
<th>Current bit</th>
<th>Previous bit</th>
<th>Operation</th>
<th>Reason</th>
</tr>
</thead>
<tbody>
<tr>
<td>a_i</td>
<td>a_{i-1}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

10. The representation of a IEEE 754 single precision floating-point number is shown below:

<table>
<thead>
<tr>
<th>sign</th>
<th>exponent</th>
<th>significand</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 bit</td>
<td>8 bits</td>
<td>23 bits</td>
</tr>
</tbody>
</table>

(a) (3%) What normalized decimal number does the following number represent:

1 0 1 1 1 1 1 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

(b) (3%) Show the representation of the number $-7.75_{10}$.

11. (6%) List three overhead items incurred in a pipelined design, and give their proper explanations.

12. (10%) Assume that increasing the first-level cache size from 16 KB to 32 KB reduces the miss rate from 3.0% to 2.0%. Suppose the machine with the 32 KB cache has a clock time of 2 ns, while the machine with 16 KB cache has a clock time of 1.6 ns. We also assume that the CPI without memory stalls, C, is the same for these two machines. Let the miss penalty to the secondary cache be 20 ns and every instruction have 1.5 memory references (1 instruction reference and 0.5 data references). Let $I$ stand for the number of instructions per program. Which machine is faster?

13. (9%) Based on the following figure, describe the operating steps of R-type (register) instructions and lw (load word) instructions.